REMARKS

The rejections presented in the Office action dated May 12, 2004 have been considered. Claims 1-3, 5-20 and 22 remain pending in the application. Reconsideration and allowance of the application as amended is respectfully requested.

Claims 5, 11, and 18 are objected to because of informalities listed in paragraph 1) of the Office Action. The undersigned attorney apologizes for failing to respond to these objections in the previous response, and submits that the failure to previously respond to these objections was an oversight. Claims 5, 11, and 18 have been amended to address the Examiner's objections, and the Applicants respectfully submit that the objection to Claims 5, 11, and 18 has now been properly addressed.

Claims 1-3, 5-7, 11-12, 14-15, 17-20, and 22 stand rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,509,119 to La Fetra. The Applicants respectfully traverse the rejection as set forth below.

Claim 1 includes performing a first comparison (e.g., using fast hit address compare (*e.g.,* 504) of the memory access address (*e.g.,* 502) to the stored tag address (*e.g.,* from tag ram 500), without regard to any error correction code associated with the stored tag address, to determine whether the requested data is stored in the cache memory. Only the requested address and the cached address are compared by fast hit address compare 504 to determine a cache hit. Claim 1 has been amended to indicate that only the addresses are compared, and no ECC comparison is performed. Any error correction data that may be associated with the cached address is disregarded for purposes of the comparison.

In contrast, both comparisons performed by La Fetra utilize error correction data that is associated with the stored tag address to determine whether the requested data is stored within cache memory. With regard to La Fetra's first comparison, La Fetra indicates that the La Fetra system uses the tag comparator 225 as was described in La Fetra's FIG. 2. FIG. 2 of La Fetra indicates that ECC data 213 and stored tag address 211 must be used to determine the value of true hit 225. More particularly, FIG. 2 as the associated description (col. 3, line 56 through col. 4, line 17) establishes that the stored tag address 211 must first be checked with associated ECC 213 and corrected if necessary prior to comparison with tag 201. If the checked/corrected stored address tag 221 matches tag 201, true hit 225 is asserted,

otherwise, true hit 225 is deasserted. Either way, stored tag address 211 and its associated error correction code ECC 213 are utilized to determine the value of true hit 225, which is in contrast to Applicants' claimed invention.

Similarly with regard to La Fetra's second comparison, assertion or deassertion of fast hit signal 407 requires not only the use of the stored address tag 213 and its associated error correction code ECC 213, but also the use of a CPU tag and a derived CPU tag ECC. In particular, with respect to FIG. 4 and associated text in column 5, lines 2-16, second comparator 401 compares the cache tag/cache tag ECC pair from cache RAM 205 with the CPU tag/derived CPU tag ECC that is generated by ECC GEN 405. Only when *both* of the comparisons match, i.e., the comparison of the cache tag with the CPU tag and the comparison of the cache tag ECC with the derived CPU tag ECC, will fast hit signal 407 be asserted (see col. 5, lines 15-16).

Thus, both of La Fetra's determinations as to whether the requested data is stored in the cache memory, i.e., true hit 225 and fast hit 407, requires at least the use of a stored tag address and its associated error correction code, and requires the additional use of the cache tag ECC with the derived CPU tag ECC in the case of fast hit 407. Claim 1 requires no ECC comparisons to issue a fast cache hit result, whereas the teaching of La Fetra differs in at least this respect. Applicants respectfully submit, therefore, that Claim 1 is not in anticipated by La Fetra.

The Applicants have reviewed the "***Response to Arguments***" relating to the Applicants' previous response to the first Office Action. The Examiner has indicated that La Fetra includes two comparisons, including a comparison of the Cache-tag/CPU-tag, and a comparison of the Cache-ECC/CPU-ECC. The Applicants have also noted the Examiner's statement relating to "separate" address and ECC comparisons. However, not only does Claim 1 indicate that a fast path comparison occurs without regard to any error correction code accompanying the stored tag address, the Applicants submit that the claim language "utilizing results of the first comparison" indicates that the results of the address comparison (*i.e.*. the address comparison without regard to any ECC) is what is used to determine whether the requested data is stored in the cache memory. In other words, it is respectfully submitted that La Fetra bases any such determination on a comparison of ***both*** address and ECC

information, while the claimed invention makes a fast path determination solely on the address information. The Applicants respectfully submit that this differs from the teaching of La Fetra.

In order to facilitate prosecution of this application, Claim 1 has been amended to more clearly set forth this distinction. Thus, if no tag address error is detected in the stored tag address, results of the first comparison of only the memory access address and the stored tag address are utilized to determine whether the requested data is stored in the cache memory. It is believed that this addresses the Examiner's comments, and more clearly sets forth what is used to establish the fast path hit/miss results for purposes of Claim 1. In view of these remarks, it is respectfully submitted that Claim 1 is not anticipated by La Fetra.

For at least the reasons set forth above, the Applicants respectfully submit that Claim 1 as presented is not anticipated by La Fetra, and is in condition for allowance.

Dependent Claims 2-3 and 5-7, which are dependent from independent Claim 1, are also rejected under 35 U.S.C. §102(b) as being unpatentable over La Fetra. It is believed that these rejections are moot in view of the remarks made in connection with independent Claim 1. These dependent claims include all of the limitations of Claim 1 and any intervening claims, and recite additional features which further distinguish these claims from the cited references. Therefore, dependent Claims 2-3 and 5-7 are also in condition for allowance.

Further, as to Claim 2, the Applicants previously amended Claim 2 and argued that the amendments to Claim 2 more particularly set forth an embodiment where monitoring for errors in the stored tag address involves identifying an error using "a **single** ECC" associated with the stored tag address. In the Examiner's "***Response to Arguments***," the Examiner notes that "two comprises one, although two may not comprise *only* one." The point is well taken, but the Applicants respectfully submit that the language "a single one" is synonymous with "only one." It therefore follows that two may not comprise a single one. Because the teaching and fundamental principle of La Fetra is to split the ECC into multiple parts, La Fetra does not teach monitoring for errors in the stored tag address involves identifying an error using a single ECC associated with the stored tag address. For at least this additional reason, it is believed that Claim 2 is in condition for allowance.

The Applicants have also amended independent Claim 11 to address the rejection similarly to that of Claim 1. The first address compare module is coupled to the tag memory to receive a tag address and to compare only the tag address to a requested address, rather than comparing ECC information as in La Fetra. Further, Claim 11 has been amended to set forth that the gated output module outputs a fast hit indication if the requested address is stored in the tag memory as determined by the comparison of only the tag address and the requested address. As previously indicated, this is not taught by La Fetra, and thus La Fetra does not anticipate Claim 11. Analogous amendments have been made to independent Claim 18, and the same rationale applies. Reconsideration and allowance of independent Claims 11 and 18 is therefore respectfully requested.

Dependent Claims 12, 14-15, 17, and 19-20, which are dependent from independent Claims 11 and 18, are also rejected under 35 U.S.C. §102(b) as being unpatentable over La Fetra. While Applicants do not acquiesce with the particular rejections to these dependent claims, it is believed that these rejections are moot in view of the remarks made in connection with independent Claims 11 and 18. These dependent claims include all of the limitations of the base claim and any intervening claims, and recite additional features which further distinguish these claims from La Fetra. Therefore, dependent Claims 12, 14-15, 17, and 19-20 are also in condition for allowance.

Regarding independent Claim 22, the Applicants previously contended that at least the means for coordinating timing between the first hit detection path means and the second hit detection path means is not taught by La Fetra. In the Examiner's "***Response to Arguments***," the Examiner "timing" need not be limited to the word "time" (or conjugations thereof), and that if the cache memory system "waits" for the true hit/miss this is "timing." The Applicants note that for a means plus function claim under 35 U.S.C. §112, ¶6, both the function and the structure must be considered. Thus, while the Applicants do not acquiesce with correspondence of function, the Applicants maintain the position that La Fetra simply discloses no structure to perform any such timing. In embodiments of the present invention, latches are used to establish proper timing. La Fetra does not teach any such structure. Whether the Examiner is contending that La Fetra teaches such timing function or whether the contention is that such structure is inherent in La Fetra, the Applicants submit that La Fetra

does not expressly or inherently teach any such means. For at least this reason, the Applicants respectfully contend that Claim 22 is not anticipated by La Fetra.

Claims 8-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over La Fetra. The Applicants respectfully traverse the rejection. The obviousness rejection is based on the Examiner's arguments as they pertain to Claim 1, and based on the Examiner's position of official notice of a logic gate. With respect to the arguments pertaining to Claim 1, Claims 8-10 are dependent from independent Claim 1, and as indicated above the Applicants respectfully contend that La Fetra does not teach all of the elements of Claim 1 as currently pending. Thus, while Applicants to not acquiesce that taking official notice, if proper, of a logic gate would necessarily teach or suggest all of the claimed recitations of Claims 8-10, these claims nevertheless include all of the limitations of Claim 1, and recite additional features which further distinguish these claims from La Fetra. Therefore, dependent Claims 12, 14-15, 17, and 19-20 are also in condition for allowance.

Claims 13 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over La Fetra. The Applicants respectfully traverse the rejection. The obviousness rejection is based on La Fetra as applied to Claim 11, in view of "Logic and Computer Design Fundamentals" (hereinafter "LCDF"). With respect to the arguments pertaining to Claim 11, Claims 13 and 16 are dependent from independent Claim 11, and as indicated above the Applicants respectfully contend that La Fetra does not teach all of the elements of Claim 11 as currently pending. While Applicants to not acquiesce that a combination of La Fetra and LCDF teaches all the limitations of the subject matter in Claims 13 and 16 as required by M.P.E.P. § 2143, it is respectfully submitted that a combination of such references fails to teach or suggest at least the limitations of the base claim. For example, the limitations set forth in Claim 16 set forth various latches coupled to specific compare modules and detectors to latch particular results and signals, as well as limitations when both the comparison results and the error indicator signal are passed to the gated output. Even assuming *arguendo* that a proper combination has been made, it is respectfully submitted that the combination does not teach such limitations. For at least these reasons, it is respectfully submitted that Claims 13 and 16 are not rendered obvious by a combination of La Fetra and LCDF.

The Applicants further contend that the proper motivation to combine La Fetra and LCDF have not been established. It has not been established why one of ordinary skill in the art, having La Fetra in front of him/her, would seek teachings of latch timings based on La Fetra's statement that the cache memory system "waits" for the true hit/miss signal. It is respectfully submitted that such motivation is derived from the benefit of the Applicants disclosure itself, rather than from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem. For example, if the nature of the problem is to wait for a signal, a resistor-capacitor (RC) network could be used or any other number of circuits differing from the claimed language. For at least this additional reason, it is respectfully submitted that *prima facie* obviousness is not established for Claims 13 and 16, and Claims 13 and 16 are therefore patentable over the cited combination of references.

CONCLUSION

The Applicants respectfully submit that the pending claims are patentable over the cited prior art of record, and that the application is in condition for allowance. If the Examiner believes it necessary, the undersigned attorney of record may be contacted at (651) 686-6633 (x110) to discuss any issues related to this case.

Respectfully submitted,

Date: November 12, 2004 By: _____

Steven R. Funk
Reg. No. 37,830
Crawford Maunu PLLC
1270 Northland Drive, Suite 390
St. Paul, Minnesota 55120
(651) 686-6633